Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned **"Version with markings to show changes made"**.

35 USC 103(a) claim rejections

Claims 17-25 are rejected under 35 USC 103(a) as being unpatentable over Yeh et al. (USPN 5,840,607) in view of Wang (USPN 4,992,391). This rejection is respectfully traversed.

Claim 17 distinguishes over Yeh et al. and Wang taken singly or in combination at least by reciting "a second doped polysilicon layer over and in contact with the second undoped polysilicon layer".

The Office Action indicates that although Yeh et al. do not show the second doped polysilicon layer of Applicants' claim 17, layer 20 in Fig. 5B of Wang shows this layer. This is respectfully traversed because layer 20 in Fig. 5B of Wang is a silicide layer not "doped polysilicon layer" as recited in Claim 17. It is well-known in this art that silicide and doped polysilicon are two different materials with different characteristics. Wang in column 3, lines 35-42, in reference to Fig. 2, states:

> Polysilicon layer 18 is formed as an undoped layer using conventional deposition techniques. Then, a silicide layer 20 is provided on polysilicon layer 18. The silicide may be selected from the group including $TaSi_2$, $WSi_2$, $TiSi_2$, and $MoSi_2$; $WSi_2$, the preferred silicide, is deposited, for example, in an environment including $SiH_2Cl_2$ and $WF_6$ at a temperature of approximately 600°C.

Here, Wang forms silicide layer 20 over a polysilicon layer. Clearly, Wang did not intend layer 20 to be doped polysilicon layer. This is further supported by Wang in column 3, lines 50-52 wherein Wang states:

> Polysilicon layers 18 and 22 are formed as undoped polysilicon in order to improve the adhesion of these layers to silicide layer 20.

Clearly, Wang requires the use of silicide layer, and has devised a method to improve the adhesion of the silicide layer to the adjacent polysilicon layers. This in fact is one of the objectives of Wang's invention as stated in column 2, lines 12-15. Thus, Wang, as with Yeh et al., fail to teach or suggest the "second doped polysilicon layer" recited in Applicants' claim 17.

Thus, claim 17 and its dependent claims 18-25 are allowable.

35 USC 102(b) claim rejections

Claims 26, 27, 31, and 33 are rejected under 35 USC 10b(b) as being anticipated by Wang (USPN 4,992,391). This rejection is respectfully traversed.

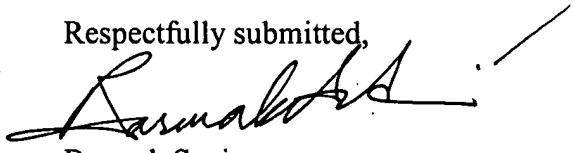
Both independent claims 26 and 33 include "a doped polysilicon layer" which, as stated above, is nowhere taught or suggested by Wang. Thus, claims 26 and 33 and their respective dependent claims 27-32 and 34-35 are allowable.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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## VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please amend claims 17, 22, 26, and 33 as follows.

17. (Amended) A semiconductor non-volatile memory cell comprising:

a first insulating layer over a substrate region;

a first doped polysilicon layer over the first insulating layer;

a first undoped polysilicon layer over and in contact with the first doped polysilicon layer, the first doped and first undoped polysilicon layers forming a floating gate;

a second insulating layer over and in contact with the first undoped polysilicon layer;

a second **[updoped]** undoped polysilicon layer over and in contact with the second insulating layer; and

a second doped polysilicon layer over and in contact with the second undoped polysilicon layer, the second doped and undoped polysilicon layers forming a control gate.

22. (Amended) The memory cell of claim 17 wherein each of said first and second doped polysilicon layers **[comprises]** are in-situ doped with impurities.

26. (Amended) A semiconductor transistor comprising:

an insulating layer over a substrate region;

an undoped polysilicon layer over and in contact with the insulating layer; and

a doped polysilicon layer over and in contact with the undoped polysilicon layer, the doped and undoped polysilicon layers forming a gate of the transistor, wherein the gate is electrically accessible.

33. (Amended) A semiconductor structure comprising:

an undoped polysilicon layer;

a doped polysilicon layer in contact with the undoped polysilicon layer; and

an insulating layer in contact with the undoped polysilicon layer, wherein the undoped polysilicon layer is sandwiched between the doped polysilicon layer and the insulating layer,

wherein the doped and undoped polysilicon layers form part of a gate which is electrically accessible.